UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/623,815 | 07/21/2003 | Marco Troost | P2001,0034 | 5766 |

24131 7590 09/14/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

| EXAMINER | |
|---|---|
| NADAV, ORI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,815 | TROOST, MARCO | |
| | Examiner | Art Unit | |
| | ori nadav | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of an element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, as recited in claim 1, are unclear as to what is meant by the phrase "for the signal and to the supply potential".

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4-10, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chrysostomides et al. (5,646,434).

Chrysostomides et al. teach in figure 5 and related text a semiconductor component comprising: a semiconductor body 1 including an electronic circuit configured therein, said electronic circuit having a terminal for a signal to be processed, said electronic circuit having a stage connected to said terminal for the signal, said electronic circuit having a terminal for obtaining a supply potential, said terminal for obtaining the supply potential connected to said stage, said stage selected from a group consisting of an input stage and an output stage;

a first conductor track Vcc1 running outside said semiconductor body, said first conductor track connected to said terminal for the signal;

a second conductor track 24 running outside said semiconductor body, said second conductor track connected to said terminal for obtaining the supply potential;

an element 13, 16 for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential; and

a further conductor track 23 running outside said semiconductor body, said further conductor track connected to said second conductor track 24;

said element for carrying the electrostatic discharge disposed outside of said semiconductor body; and

said element for carrying the electrostatic discharge connected outside of said semiconductor body to said further conductor track and to said first conductor track.

Figure 5 does not depict a semiconductor body 30. Figure 1 of Chrysostomides et al. depicts a semiconductor body 30.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form semiconductor body 30 in the device of figure 5, in order to form the device with all its advantages as taught by Chrysostomides et al.

Regarding claims 4 and 5, Chrysostomides et al. teach in figures 1 and 5 said further conductor track 23 surrounds said semiconductor body; and bonding wires 9 and 6 of said first conductor track and said second conductor track cross said further conductor track.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend the first conductor track and the second conductor track cross said further conductor track, wherein an insulation material configured where said further conductor track crosses said first conductor track in Chrysostomides et al.'s device in order to reduce the contact resistance between the conductors and to avoid short circuit in the device, respectively.

Regarding claim 6, Chrysostomides et al. teach in figure 5 a third conductor track Vcc2; a terminal for a signal and assigned to said third conductor track; and a further element 13, 15 for carrying an electrostatic discharge; said further conductor track running in a main direction and having a conductor track portion branching away from said main direction; said third conductor track crossing said

further conductor track near said conductor track portion of said further conductor track (via wiring 8); and said conductor track portion of said further conductor track is connected to said further element for carrying the electrostatic discharge.

Regarding claims 7-8, Chrysostomides et al. teach in figure 5 a bonding wire connecting said first conductor track to said terminal for the signal; and a bonding wire connecting said second conductor track to said terminal for obtaining the supply potential, wherein

said terminal for the signal and said terminal for obtaining the supply potential are metallized areas configured in said semiconductor body.

Regarding claim 9, Chrysostomides et al. teach in figure 5 an input stage has at least one transistor with a gate connected to said terminal for the signal; said transistor has a drain terminal and a source terminal; said drain terminal or said source terminal of said transistor connected to said terminal for the supply potential.

Regarding claim 10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inverter as the input stage in Chrysostomides et al.'s device in order to use the device in an application which requires an inverter.

Claim 3, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chrysostomides et al. (5,646,434) in view of Kohama (5,917,362).

Chrysostomides et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a package surrounding said semiconductor body and said further conductor track; said package partially surrounding said first conductor track such that a portion of said first conductor track facing toward said semiconductor body runs inside said package and a portion of said first conductor track facing away from said semiconductor body runs outside said package; and

said package partially surrounding said second conductor track such that a portion of said second conductor track facing toward said semiconductor body runs inside said package and a portion of said second conductor track facing away from said semiconductor body runs outside said package.

Kohama teaches in figure 18 and related text a package 211 surrounding a semiconductor body and a further conductor track; said package partially surrounding a first conductor track such that a portion of said first conductor track facing toward said semiconductor body runs inside said package and a portion of said first conductor track facing away from said semiconductor body runs outside said package; and

said package partially surrounding a second conductor track such that a portion of said second conductor track facing toward said semiconductor body runs

inside said package and a portion of said second conductor track facing away from said semiconductor body runs outside said package.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a package surrounding said semiconductor body and said further conductor track; said package partially surrounding said first conductor track such that a portion of said first conductor track facing toward said semiconductor body runs inside said package and a portion of said first conductor track facing away from said semiconductor body runs outside said package; and

said package partially surrounding said second conductor track such that a portion of said second conductor track facing toward said semiconductor body runs inside said package and a portion of said second conductor track facing away from said semiconductor body runs outside said package.

Claim 3, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chrysostomides et al. (5,646,434) in view of Reczek (5,426,323).

Chrysostomides et al. teach substantially the entire claimed structure, as applied to claim 1 above, except said element for carrying the electrostatic discharge is a diode; said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track.

Reczek teaches in figure an element for carrying the electrostatic discharge is a diode; said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a diode as the element for carrying the electrostatic discharge, wherein said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track in Chrysostomides et al.'s device in order to provide protection to the device.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
9/9/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800